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3rd International Conference on Through-life Engineering Services  
**The design of reliable circuits using logic redundancy**

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## Abstract

With the increasing demand for more durable products, the necessity of designing more resilient products is evident. When it comes to electronic systems, many strategies have been applied to enhance the durability and performance of the operating circuits. For a long time, the main focus was to develop increasingly reliable components, however, yield enhancement techniques may not be sufficient for future technologies. As a solution to this, redundancy strategies are being introduced in order to regain reliability of circuits even if the individual components are not as reliable as desired. The use of logic redundancy and series or parallel association of transistors is proposed as a strategy in the design of fault tolerant logic gates (that are the basic elements of many complex computing structures), such as NAND and NOR. Fault injection simulations show that the reliability of these gates in the presence of random stuck-at faults may be increased by our design approach and that the strategy is extensible to more elaborate circuits.

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**Keywords:** Reliability; redundancy; logic gates; transistor failure.

## 1. Introduction

Products that are prone to fail may either tarnish the reputation of a company or cause loss of profit, particularly when it comes up to technological goods. Since they are expected to keep working properly for some years, consumer satisfaction and loyalty is directly tied to through-life reliability. For example, two leading computing companies Apple and Microsoft had problems concerning the computer Apple III and the operational system Windows Vista, respectively. Both products presented serious flaws and, as a consequence, the sales of these products were dramatically lower than expected, demanding that the next generation products were quickly released. Besides, in the case of a product to which people entrust their lives, failures may be fatal. Therefore, it is important to assure that a designed product will have a reasonable life span, according to its usage, in other words, to have reliability[1].

Currently, many products (or parts of products) depend on an electronic circuit. However, unlike mechanical structures, it is hard to detect flaws in circuits. Thus, it may be necessary to replace a whole component due to a single device that is not working properly. In some cases, it is better to replace than to pay for a more reliable device; in others, however, a high reliability is required by the customer or replacing is not

always feasible (in satellites or military weapons, for instance).

In these situations, it is necessary that the circuit keeps working. Due to all these reasons, developing strategies so as to design more reliable circuits is extremely important nowadays.

When it comes to designing a more reliable system, many strategies are used. For instance, one can develop more resistant devices (which leads to more resistant circuits), embed physical structures to help heat dissipation (thus, increasing devices lifespan) or use defect avoidance (averting failures to occur). Yet, the main approach, that will be more deeply investigated in this research, is redundancy (“the existence of more than one mean of performing its function”[1]), pointing towards self-repairing techniques. In this case, the idea is that the circuit may continue working even if some devices stop working, by having more than one structure that can perform the same function and (in the more advanced situations) repair the the flaw. Being able to repair, even though being a complex process, eases one of the biggest problems regarding redundancy: increase of costs and occupied space (since redundant circuits uses more devices to perform the same task). Nevertheless, the study of self-repairing circuits is still incipient (its applications are few yet) and there is some dependence on redundancy, anyway. Therefore, it is evident that the redundancy and self-repairing circuits are important issues at the moment.

## 2. Transistor reliability

Transistors, surely, are one of the most important devices used currently. It can be noticed in [2] that, indeed, the semiconductor business is of a massive importance in the electronics field since the 1990's. That is because they are largely used in integrated circuits, the base for lots of circuits used nowadays. And when it comes to logic and memory devices, transistors are the basic element (and in this project, they will be largely used). Therefore, in order to realise more reliable circuits, it would be desired more reliable transistors. One option would be purchase or develop ultra-resistant devices, as shown in [3], for example. Indeed, each time these components are manufactured at a smaller scale, it is necessary to guarantee that they will still work. So this approach is really important. Nevertheless, redundancy can be helpful as well. In fact, in [4], it is proposed how to modify the failure probability of transistors using parallel (figure 1) and series (figure 2) association of transistors. Obviously, according to what is the behaviour of the circuit, a certain kind of association will lead to better results. So, certainly, redundancy is a strategy that is already known so as to enhance a single transistor performance.

Basically the circuits analysed on this work are logic gates, that are made out of transistors. Therefore, it is important to make a numerical analysis of the failure rates of these components. For doing that, the following assumptions were made, to which the results are constrained:

- A failure occurs when, in a certain moment, the output would not be correct for at least one of the possible inputs (not only whether the output is right or not);
- The failure modes considered are basically open and short circuit between collector and emitter (stuck-at-fault model);
- The failure of each device is independent of the others;
- Components that represent the same device have the same failure probabilities;
- If a short and an open failure (they are independent) occur for the same device, the resultant failure is an open circuit;
- Delays or noises do not interfere on the failure rate.

Some of these assumptions were based on the work "Logic Gate Failure Characterization for Nanoelectronic EDA Tools"[4]. However, some assumptions are different, mainly the fifth item. By assuming that, the probability of a short failure to happen will numerically reduce, since a short can only happen if there is no open, whereas the probability of an open failure remains the same. Therefore, the results found will be different as well.

## 3. Enhanced NAND gate

The circuit shown in figure 3 corresponds to the traditional NAND gate. For it to work, it is necessary that both transistors are operating properly. Therefore, the failure rate is given by equation 1 (where  $p_o$  and  $p_s$  are the probabilities of an open and a short fault occur, respectively, in one single transistor).

$$FR = 1 - (1 - p_o)^2(1 - p_s)^2 \quad (1)$$

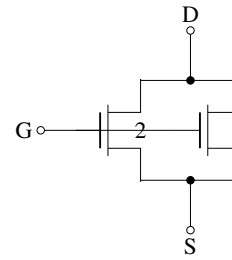


Figure 1. Parallel Association of 2 Transistors.

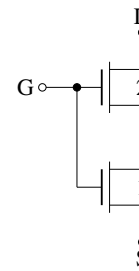


Figure 2. Series Association of 2 Transistors.

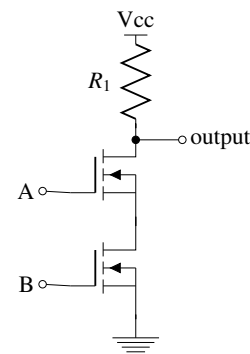


Figure 3. Traditional NMOS NAND gate.

The circuit shown in figure 4 is the proposed enhanced NAND gate using redundancy. However, each transistor, actually, represents two transistors in parallel (as in figure 1).

A transistor model was created using the Simulink platform in MATLAB and simulations were run considering the presence of random stuck-at-fault errors. The results are shown in table 1, whereby it can be noticed that the results from the MATLAB simulation for the traditional NAND gate roughly agree with the theoretical values from equation 1. This brings credibility to the construction used in the simulation and, thus, allows its use for the analysis of a more complex system (that is the enhanced gate). Therefore, since the results in the last column of this table suggest that the proposed redundant circuit is more reliable than the traditional one (up to  $10^2$  times more), the proposed structure is, indeed, less prone to fail.

Adding more transistors (six times more in this case) makes the circuit bigger. Moreover, in this construction the processing time may increase, since it consists of a serial configuration. However, if the goal is to make a more reliable component, this is an acceptable trade-off.

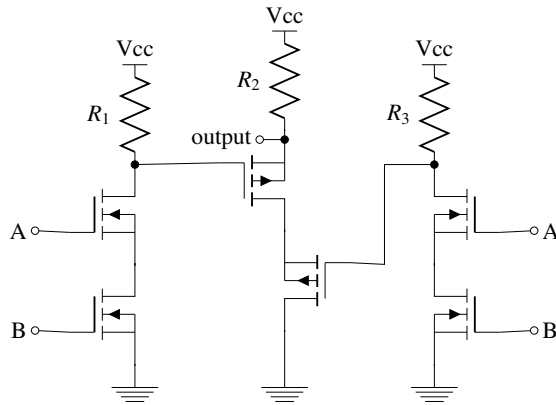


Figure 4. Enhanced NMOS and PMOS NAND gate.

Table 1. Comparison between failure rates of traditional and enhanced NAND gates - average simulations results using  $10^5$  samples.

$p_o = p_s$	Traditional (Theory)	Traditional (MATLAB)	Enhanced (MATLAB)
$1 \times 10^{-4}$	$4.00 \times 10^{-4}$	$4 \times 10^{-4}$	0
$5 \times 10^{-4}$	$2.00 \times 10^{-3}$	$2 \times 10^{-3}$	$1 \times 10^{-5}$
$1 \times 10^{-3}$	$3.99 \times 10^{-3}$	$4 \times 10^{-3}$	$3 \times 10^{-5}$
$5 \times 10^{-3}$	$1.99 \times 10^{-2}$	$2 \times 10^{-2}$	$6 \times 10^{-4}$
$1 \times 10^{-2}$	$3.94 \times 10^{-2}$	$4 \times 10^{-2}$	$2 \times 10^{-3}$
$2.5 \times 10^{-2}$	$9.63 \times 10^{-2}$	$1 \times 10^{-1}$	$2 \times 10^{-2}$
$5 \times 10^{-2}$	0.185	0.18	$6 \times 10^{-2}$
0.1	0.344	0.32	0.19

#### 4. Enhanced NOR gate

The circuit in figure 5 corresponds to the traditional NOR gate. For it to work, it is necessary that both transistors are operating properly. Therefore, the failure rate is the same as shown in equation 1. The circuit in figure 6 corresponds to the enhanced NOR gate. Nevertheless, each transistor corresponds to two transistors in series (as in figure 2).

Using the same transistor model in the Simulink platform in MATLAB, simulations were run considering the presence of random stuck-at-fault errors. The results are shown in table 2, whereby it can be noticed again that the results from the MATLAB simulation for the traditional NOR gate roughly agree with the theoretical values, reinforcing the credibility of the construction used in the simulation. Therefore, the results

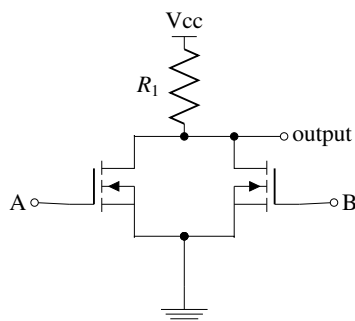


Figure 5. Traditional NMOS NOR gate.

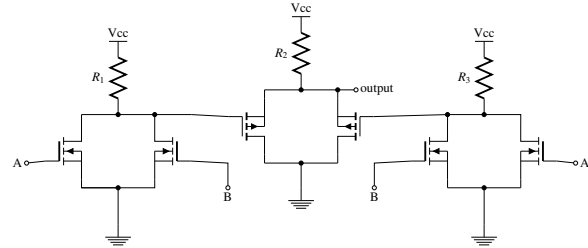


Figure 6. Enhanced NMOS and PMOS NOR gate.

Table 2. Comparison between failure rates of traditional and enhanced NOR gates - average simulations results using  $10^5$  samples.

$p_o = p_s$	Traditional (Theory)	Traditional (MATLAB)	Enhanced (MATLAB)
$1 \times 10^{-4}$	$4.00 \times 10^{-4}$	$4 \times 10^{-4}$	0
$5 \times 10^{-4}$	$2.00 \times 10^{-3}$	$2 \times 10^{-3}$	$1 \times 10^{-5}$
$1 \times 10^{-3}$	$3.99 \times 10^{-3}$	$4 \times 10^{-3}$	$3 \times 10^{-5}$
$5 \times 10^{-3}$	$1.99 \times 10^{-2}$	$2 \times 10^{-2}$	$6 \times 10^{-4}$
$1 \times 10^{-2}$	$3.94 \times 10^{-2}$	$4 \times 10^{-2}$	$2 \times 10^{-3}$
$2.5 \times 10^{-2}$	$9.63 \times 10^{-2}$	$1 \times 10^{-1}$	$2 \times 10^{-2}$
$5 \times 10^{-2}$	0.185	0.18	$7 \times 10^{-2}$
0.1	0.344	0.32	0.21

in the last column of this table once more suggest that the proposed redundant circuit is, indeed more reliable than the traditional one.

In the same way as in the NAND gate, there is a trade-off in this NOR gate, that involves using six times more transistors and using a serial configuration (increasing processing time). Again, an acceptable trade-off to achieve reliability.

#### 5. Conclusion

In this work, it has been proposed models based on logic redundancy and parallel or series transistor association that increase the reliability of two logic gates: NAND and NOR. Computer simulations using MATLAB show that the studied circuits may be more tolerant to stuck-at-fault failures than the traditional circuits used to implement such logic functions, using only six times more MOS transistors. Since the basic digital circuits (logic gates) can be made more resilient, so can more complex structures which are made out of these simple ones. Therefore, the same strategy may be applied to more elaborate circuits. Moreover, in the continuation of this work, it will be analysed further the behaviour of the failure rates when  $p_s$  and  $p_o$  are not the same and a more general analytical reliability analysis for the proposed enhanced gates.

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